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EXAMINER	
MAGEE, THOMAS J	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/776,375	ENOMOTO, YOSHIYUKI	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 6, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (6,468,894 B1).

3. Regarding Claim 1,Yang et al. disclose a semiconductor device comprising:

a first buried wiring (14) (Figure 7),

a second buried wiring (28) formed as a layer different from said first buried wiring,

a contact hole (30), which is formed between said first buried wiring and said second buried wiring and is filled with a wiring material for electrically connecting said first buried wiring and said second buried wiring therethrough, and

a dummy hole (34, 36) is so formed in vicinity of first buried wiring and is filled with wiring material therein.

Yang et al. do not disclose that the diameter of the dummy hole is different from that of said contact hole. Parameters such as diameters of via holes (contact and dummy) in the art of semiconductor manufacturing are subject to routine experimentation and optimization to

achieve the desired quality during fabrication. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate sizes of vias within the claimed values to form a high quality film.

4. Regarding Claim 2, Yang et al. disclose a semiconductor device wherein said second buried layer (28) is formed as an upper layer of said first buried wiring (14), and said dummy hole is formed "over" said first buried wiring.

Yang et al. do not disclose that the diameter of the dummy hole is larger than that of said contact hole. Parameters such as diameters of via holes (contact and dummy) in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired quality during fabrication. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate sizes of vias within the claimed values to form a high quality film.

5. Regarding Claim 3, Yang et al. disclose a semiconductor device wherein said second buried wiring (14) is formed as an upper layer of said first buried wiring (28) and said dummy hole (34) is formed below said first buried wiring. That is, the terms, "upper" and "below" are merely relative terms that do not structurally distinguish the claims from Yang et al.

Yang et al. do not disclose that the diameter of the dummy hole is smaller than that of said

contact hole. Parameters such as diameters of via holes (contact and dummy) in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired quality during fabrication. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate sizes of vias within the claimed values to form a high quality film.

6 Regarding Claim 4, Yang et al. disclose that second buried wiring (14) is formed as a lower layer of said first buried wiring (28, and said dummy hole (34) is formed below said first buried wiring.

Yang et al. do not disclose that the diameter of the dummy hole is smaller than that of said contact hole. Parameters such as diameters of via holes (contact and dummy) in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired quality during fabrication. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate sizes of vias within the claimed values to form a high quality film.

7 Regarding Claim 5, Yang et al. disclose that second buried layer (28) is formed as an upper layer of said first buried wiring (14), and said dummy hole (36) is formed over said first buried wiring.

Yang et al. do not disclose that the diameter of the dummy hole is smaller than that of said

contact hole. Parameters such as diameters of via holes (contact and dummy) in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired quality during fabrication. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate sizes of vias within the claimed values to form a high quality film.

8 Regarding Claim 6, Yang et al. disclose that the wiring material is made of copper (Col.3, lines 56 – 57) (Col. 5, lines 19 – 20).

9 Regarding Claim 10, Yang et al. disclose a method for manufacturing a semiconductor device including a first buried wiring (14), a second buried wiring (28) formed as an upper layer of said first buried wiring, a contact hole, which is formed between said first buried wiring and said second buried wiring and is filled with a wiring material for permitting electric connection between said first buried wiring and said second buried wiring therewith, and a dummy hole (36) which is formed over first buried wiring in the vicinity of said contact hole and is filled with wiring material therein, the method comprising the steps of:

Forming said first buried wiring (14),

forming an insulating film (17,18) on said first buried wiring through a diffusion preventive film (Figure 2) and etching the insulating film to simultaneously form said contact hole and dummy hole in said insulating film (Figure 3) so that a surface of said first buried wiring (14) is exposed to a bottom of said dummy hole.(36), and

filling said contact hole and said dummy hole with wiring material, respectively (Figure 4).

Yang et al. do not disclose that the diameter of the dummy hole is larger than that of said contact hole. Parameters such as diameters of via holes (contact and dummy) in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired quality during fabrication. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate sizes of vias within the claimed values to form a high quality film.

10 Claims 7 –9, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al., as applied to Claims 1 – 6, and 10, and further in view of Prior Art of the instant application.

11. Regarding Claims 7 – 9, Yang et al. do not disclose that a plugging failure is caused by filling a dummy hole of a "selected" size with wiring material. However, the Admitted Prior Art (Background) section (pp. 3 – 4) of the instant application discloses that for copper wiring and certain sizes, a voiding of the copper occurs, resulting in "voiding" and "electrical connection interruption" (plugging failure).
It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Yamaha et al. with known prior art as presented in the instant application to produce a device wherein defect (void) nucleation was reduced.

12. Regarding Claim 11, Yang et al. disclose a method for manufacturing a semiconductor

device including a first buried wiring (28), a second buried wiring (14) formed as a lower layer of said first buried wiring, a contact hole (30) which is formed between said first buried wiring and said second buried wiring and is filled with a wiring material for electrically connecting said first buried wiring and said second buried wiring therewith, and a dummy hole (34) which is formed below first buried wiring (28) in the vicinity of said contact hole and is filled with wiring material therein. The terms, "upper" and "below" are merely relative terms that do not structurally distinguish the claims from Yang et al.

The method comprises the steps of:

forming a wiring groove for forming said first buried wiring (28) and forming said dummy hole (34) below the wiring groove,

burying said dummy hole and said wiring groove with wiring material (See Figure 7), and

forming the contact hole (30) formed by burying of the wiring material and filling said contact hole with wiring material.

Yang et al. do not disclose that the diameter of the dummy hole is smaller than that of said contact hole. Parameters such as diameters of via holes (contact and dummy) in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired quality during fabrication. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate sizes of vias within the claimed values to form a high quality film.

Yang et al. do not disclose that a plugging failure is caused by filling a dummy hole of a "selected" size with wiring material. However, the Admitted Prior Art (Background) section (pp. 3 – 4) of the instant application discloses that for copper wiring and certain sizes, a voiding of the copper occurs, resulting in "voiding" and "electrical connection interruption" (plugging failure). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Yamaha et al. with known prior art as presented in the instant application to produce a device wherein defect (void) nucleation was reduced.

13. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. in view of Yamaha et al. (US 5,885,857) and Prior Art of the instant application.

14. Regarding Claim 12, Yang et al. disclose a method for manufacturing a semiconductor device including a first buried wiring (28), a second buried wiring (14) formed as a lower layer of said first buried wiring, a contact hole which is formed between said first buried wiring and said second buried wiring and is filled with a wiring material for electrically connecting said first buried wiring and said second buried wiring therewith; and a dummy hole (34) which is formed below first buried wiring (28) in the vicinity of said contact hole and is filled with wiring material therein, the method comprising the steps of:

forming said first buried wiring (28),

forming said contact hole (30) and said contact hole over said second buried wiring (14),

forming a groove for wiring said first wiring (28) and

filling a wiring material in said contact hole, said dummy hole, said groove for wiring, respectively.

Yang et al. do not disclose that the diameter of the dummy hole is smaller than that of said contact hole. Parameters such as diameters of via holes (contact and dummy) in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired quality during fabrication. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate sizes of vias within the claimed values to form a high quality film.

Yang et al. do not disclose that a plugging failure is caused by filling a dummy hole of a "selected" size with wiring material. However, the Admitted Prior Art (Background) section (pp. 3 – 4) of the instant application discloses that for copper wiring and certain sizes, a voiding of the copper occurs, resulting in "voiding" and "electrical connection interruption" (plugging failure). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Yamaha et al. with known prior art as presented in the instant application to produce a device wherein defect (void) nucleation was reduced.

Further, Yang et al. do not disclose that the buried wiring is electrically connected to both the contact hole and dummy hole. Yamaha et al. disclose (Col 10, lines 35 – 41) that the dummy wiring pattern can be generated using gate electrode material (Figure 2) extending to the peripheral region, wherein the contact hole (over device) region is electrically connected

to the dummy hole region. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Yamaha et al. with Yang et al. to obtain a more efficient manufacturing procedure.

15. Regarding Claim 13, Yang et al. disclose a method for manufacturing a semiconductor device including a first buried wiring (14), a second buried wiring (28) formed as an upper layer of said first buried wiring, a contact hole, which is formed between said first buried wiring and said second buried wiring and is filled with a wiring material for electrically connecting said first buried wiring and said second buried wiring therewith, and a dummy hole (36) which is formed over first buried wiring in the vicinity of said contact hole and is filled with wiring material therein, the method comprising the steps of:

forming said first buried wiring (14),

forming said contact hole (36) and a dummy pattern over said first buried wiring (14),

forming a groove for wiring over said first wiring (11a) for forming second buried wiring (28), and

filling a wiring material in said contact hole, said dummy hole, said groove for wiring, respectively. (See Figure 7).

Yang et al. do not disclose that the diameter of the dummy hole is smaller than that of said contact hole. Parameters such as diameters of via holes (contact and dummy) in the art of semiconductor manufacturing are subject to routine experimentation and optimization to achieve the desired quality during fabrication. Therefore, it would have been obvious to one of

ordinary skill in the art at the time of the invention to incorporate sizes of vias within the claimed values to form a high quality film.

Yang et al. do not disclose that a plugging failure is caused by filling a dummy hole of a "selected" size with wiring material. However, the Admitted Prior Art (Background) section (pp. 3 – 4) of the instant application discloses that for copper wiring and certain sizes, a voiding of the copper occurs, resulting in "voiding" and "electrical connection interruption" (plugging failure). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Yamaha et al. with known prior art as presented in the instant application to produce a device wherein defect (void) nucleation was reduced.

Further, Yang et al. do not disclose that the buried wiring is electrically connected to both the contact hole and dummy hole. Yamaha et al. disclose (Col 10, lines 35 – 41) that the dummy wiring pattern can be generated using gate electrode material (Figure 2) extending to the peripheral region, wherein the contact hole (over device) region is electrically connected to the dummy hole region. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Yamaha et al. with Yang et al. to obtain a more efficient manufacturing procedure.

Conclusions

16. Any inquiry concerning this communication or earlier communications from the Examiner

should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
April 25, 2005

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